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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,113	08/28/2003	Aveek Sarkar	004-8907	7868
66083 7590 03/28/2007 SUN MICROSYSTEMS, INC. c/o DORSEY & WHITNEY, LLP 370 SEVENTEENTH ST.			EXAMINER	
			SANDOVAL, PATRICK	
SUITE 4700 DENVER, CO 80202 ART UNIT PAPER I				PAPER NUMBER
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SHORTENED STATUTORY	PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

		Application No.	Applicant(s)				
Office Action Summary		10/651,113		SARKAR ET AL.			
		Examiner	Art Unit				
		Patrick Sandoval	2825				
Period fo	The MAILING DATE of this communication Reply	on appears on the cover s	heet with the correspondence a	ddress			
WHIC - Exte after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR FOR EVER IS LONGER, FROM THE MAILIN nsions of time may be available under the provisions of 37 C SIX (6) MONTHS from the mailing date of this communicati period for reply is specified above, the maximum statutory are to reply within the set or extended period for reply will, by reply received by the Office later than three months after the ed patent term adjustment. See 37 CFR 1.704(b).	NG DATE OF THIS CON FR 1.136(a). In no event, however on. period will apply and will expire SI statute, cause the application to h	MMUNICATION. er, may a reply be timely filed X (6) MONTHS from the mailing date of this second ABANDONED (35 U.S.C. & 133)				
Status							
1)	Responsive to communication(s) filed on	02 January 2007, claim	20 was cancelled				
2a)□		This action is non-final.					
3)	==-/ -						
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Dispositi	on of Claims	• •					
4)⊠	Claim(s) 1-28 and 30-42 is/are pending in	the application					
	4a) Of the above claim(s) is/are with	• •	ion				
	Claim(s) is/are allowed.						
	Claim(s) <u>1-16,18-34 and 36-42</u> is/are reje	cted.					
	Claim(s) 17 and 35 is/are objected to.						
	Claim(s) are subject to restriction a	and/or election requirement	ent.				
	on Papers	·	-				
	The specification is objected to by the Exa	miner					
	The drawing(s) filed on is/are: a)		sted to by the Everniner	•			
	Applicant may not request that any objection to						
	Replacement drawing sheet(s) including the co			CED 4 404/4)			
11)	The oath or declaration is objected to by the						
	inder 35 U.S.C. § 119			10 102.			
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	Acknowledgment is made of a claim for fo ☐ All b) ☐ Some * c) ☐ None of:	reign priority under 35 U	.S.C. § 119(a)-(d) or (f).				
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	1. Certified copies of the priority documents have been received.						
	 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage 						
	application from the International Bi			i Stage			
* S	ee the attached detailed Office action for						
	and and the detailed office action for a	a nacor the certified copi	es not received.				
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	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-94)	4) ∐ Int B) Pa	erview Summary (PTO-413) per No(s)/Mail Date				
i) 🔲 Inform	nation Disclosure Statement(s) (PTO/SB/08) No(s)/Mail Date		tice of Informal Patent Application				

DETAILED ACTION

1. This Office Action responds to Applicant's amendment and drawing filed on 1/02/2007. Claims 1-42 are pending, wherein claims 1, 12, 22-28 and 36-37 have been amended. Claim 29 has been cancelled.

Response to Amendment

2. Applicant's arguments, see Remarks Pages 10-12, filed 1/2/2007, with respect to the rejection(s) of claim(s) 1-9, 12-15, 18-19, 22-33 and 36-42 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made with respect to claims 1-16, 18-28, 30-34 and 36-42 in view of Kovacs-Birkas et al. (Kovacs-Birkas) (US 7,149,991) under 35 USC 102(e).

Claim Objections

3. Claims 12, 17 and 35 are objected to because of the following informalities: In claim 12, replace "course" in line 8 with –coarse--.

In claim 17, line 6, delete "about" because the term would render the claim indefinite.

In claim 35, line 7, delete "about" because the term would render the claim indefinite.

4. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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- 6. Claims 1-16, 18-28, 30-34 and 36-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Kovacs-Birkas et al. (Kovacs-Birkas) (US 7,149, 991).
- 7. **Pursuant to claims 1, 22 and 37**, Kovacs-Birkas discloses a method for predicting the timing response of a circuit path, a computer readable medium product and a system for performing the method, the method comprising:

obtaining a first estimated timing response of a first circuit path using a first timing model (Kovacs-Birkas, Col. 7, II. 39-67, Col. 8, II. 1-58, Fig. 3);

obtaining a second estimated timing response of the first circuit path using a second timing model (Kovacs-Birkas, Col. 7, II. 39-67, Col. 8, II. 1-58, Fig. 3);

generating a correction factor based on a variation between the first estimated timing response and the second estimated timing response (Kovacs-Birkas, Col. 7, II. 39-67, Col. 8, II. 1-58, Fig. 3); and

applying the correction factor to the first timing model (Kovacs-Birkas, Col. 7, II. 39-67, Col. 8, II. 1-58, Fig. 3).

8. **Pursuant to claims 2, 23 and 38**, Kovacs-Birkas discloses comprising obtaining estimated timing responses of a plurality of circuit paths using the first timing model (Kovacs-Birkas, Col. 2, II. 28-67, Col. 3, II. 1-17, Fig. 1, Fig. 3).

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9. **Pursuant to claim 3, 24, 25 and 39**, Kovacs-Birkas discloses selecting the first circuit path from the plurality of circuit paths, wherein applying the correction factor to the first timing model includes adjusting the estimated timing responses of the plurality of circuit paths based on the correction factor (Kovacs-Birkas, Col. 7, II. 39-67, Col. 8, II. 1-58, Fig. 3).

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- 10. **Pursuant to claims 4, 26 and 40**, Kovacs-Birkas discloses comprising generating a netlist describing the plurality of paths (Kovacs-Birkas, Col. 7, II. 22-38).
- 11. **Pursuant to claim 5 and 27,** Kovacs-Birkas discloses wherein the step of obtaining a second estimated timing response includes providing the netlist to a modeling tool employing the second timing model (Kovacs-Birkas, Col. 7, II. 22-38).
- 12. **Pursuant to claims 6, 28 and 41,** Kovacs-Birkas discloses wherein generating a correction factor includes comparing the first estimated timing response and the second estimated timing response (Kovacs-Birkas, Col. 7, II. 39-67, Col. 8, II. 1-58, Fig. 3).
- 13. **Pursuant to claim 7 and 42,** Kovacs-Birkas discloses wherein applying the correction factor includes adjusting the first estimated timing response based on the correction factor (Kovacs-Birkas, Col. 7, II. 39-67, Col. 8, II. 1-58, Fig. 3).
- 14. **Pursuant to claims 8 and 9,** Kovacs-Birkas discloses wherein the first estimated timing response includes an estimated signal propagation delay (Kovacs-Birkas, Col. 2, II. 10-27, Col. 5, II. 66-67, Col. 6, II. 1-12).
- 15. **Pursuant to claims 10 and 20**, Kovacs-Birkas discloses wherein the correction factor includes a scaling factor (Kovacs-Birkas, Col. 10, II. 24-49).

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16. Pursuant to claims 11 and 21, Kovacs-Birkas discloses wherein the correction

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factor includes an offset (Kovacs-Birkas, Col. 9, II. 6-14).

17. **Pursuant to claims 12 and 30**, Kovacs-Birkas discloses a method for predicting the timing response of a circuit path, and a computer readable medium product for

performing the method, the method comprising:

obtaining coarse estimated timing responses for a plurality of circuit paths using a first timing model, the first timing model having a first accuracy (Kovacs-Birkas, Col. 7, II. 39-67, Col. 8, II. 1-58, Fig. 3);

obtaining refined estimated timing responses for one or more selected circuit paths of the plurality of circuit paths using a second timing model having a second accuracy greater than the first accuracy (Kovacs-Birkas, Col. 7, II. 39-67, Col. 8, II. 1-58, Fig. 3);

generating a correction factor based on the course estimated timing response of the one or more selected circuit paths and the refined timing estimates of the one or more selected circuit paths (Kovacs-Birkas, Col. 7, II. 39-67, Col. 8, II. 1-58, Fig. 3) and

adjusting the coarse estimated timing responses of the plurality of circuit paths based on the correction factor (Kovacs-Birkas, Col. 7, II. 39-67, Col. 8, II. 1-58, Fig. 3)

18. **Pursuant to claim 13 and 31**, Kovacs-Birkas discloses wherein obtaining the coarse estimated timing responses includes estimating timing responses for the plurality of circuit paths using a modeling tool employing coarse timing assumptions (Kovacs-Birkas, Col. 2, II. 28-67, Col. 3, II. 1-17, Fig. 1, Fig. 3)

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19. **Pursuant to claim 14 and 32,** Kovacs-Birkas discloses wherein obtaining refined estimated timing responses includes using a modeling tool employing refined timing assumptions (Kovacs-Birkas, Col. 2, II. 28-67, Col. 3, II. 1-17, Fig. 1, Fig. 3).

- 20. **Pursuant to claim 15 and 33**, Kovacs-Birkas discloses comprising generating a netlist describing the plurality of circuit paths (Kovacs-Birkas, Col. 7, II. 22-38).
- 21. **Pursuant to claims 16 and 34**, Kovacs-Birkas discloses wherein generating a correction factor includes determining a statistical variation between the course estimated timing response of the one or more selected circuit paths and the refined timing estimates of the one or more selected circuit paths in the generation of a correction factor (Kovacs-Birkas, Col. 6, II. 22-38).
- 22. **Pursuant to claims 18**, Kovacs-Birkas discloses wherein the coarse estimated timing responses include an estimated signal propagation delay (Kovacs-Birkas, Col. 2, II. 10-27, Col. 5, II. 66-67, Col. 6, II. 1-12).
- Pursuant to claims 19, Kovacs-Birkas discloses wherein the coarse estimated timing responses include an estimated signal propagation time (Kovacs-Birkas, Col. 2, II. 10-27, Col. 5, II. 66-67, Col. 6, II. 1-12).
- 24. **Pursuant to claim 36**, Kovacs-Birkas discloses wherein the computer readable medium is selected from a group consisting of a random access memory, a read only memory, a magnetic tape, a magnetically encodable disk, an optically encodable tape, and an optically encodable disk (Kovacs-Birkas, Col. 4, II. 64-67, Col. 5, II. 1-2, wherein a RAM, ROM magnetic tape, etc. are inherent to a computer readable medium).

Allowable Subject Matter

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- 25. Claims 17 and 35 contain allowable subject matter.
- 26. Claims 17 and 35 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 27. The following is a statement of reasons for the indication of allowable subject matter:
- 28. **Pursuant to claims 17 and 35**, in a method of designing, analyzing and comparing timing models, and a computer readable medium product for performing the method, the prior art does not fairly teach or suggest:

generating a correction factor for each of the plurality of circuit paths, wherein the statistical variation is equal to a standard deviation of the correction factors for the plurality of circuit paths divided by mean of the correction factors for the plurality of circuit paths; and

adjusting the coarse estimated timing responses of each of the plurality of circuit paths individually, if the statistical variation exceeds twenty percent.

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick Sandoval whose telephone number is 571-272-7973. The examiner can normally be reached on 8:00 am to 5:30 pm Monday through Friday.

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30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for

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the organization where this application or proceeding is assigned is 571-273-8300.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information

Patrick Sandoval **Patent Examiner**

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PRIMARY EXAMINER Paul Divl

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system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.